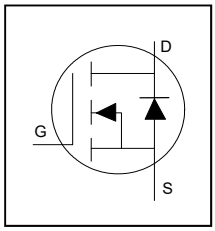
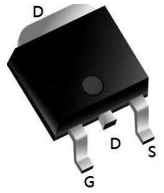
GSD90N02T

Application
- Optimized for UPS/Inverter Applications
- Low Voltage Power Tools

Benefits
- Fully Characterized Avalanche Voltage and Current
- Lead-Free, RoHS Compliant



V_{DSS}	30	V
$R_{DS(on)}$ max (@ V_{GS} = 10V)	2.4	mΩ
(@ V_{GS} = 4.5V)	3.5	
$Q_{g\ (typical)}$	40	nC
$I_{D\ (Silicon\ Limited)}$	179①	A
$I_{D\ (Package\ Limited)}$	90A	



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
GSD90N02T	D-Pak	Tape and Reel	2500	GSD90N02T

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	179①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	127①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	90	
I_{DM}	Pulsed Drain Current ②	357	
P_D @T_C = 25°C	Maximum Power Dissipation	125	W
P_D @T_C = 100°C	Maximum Power Dissipation	63	W
	Linear Derating Factor	0.83	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	——	1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	18	——	mV/°C	Reference to 25°C, I_D = 1mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	1.6	2.2	mΩ	V_{GS} = 10V, I_D = 90A ④
		——	2.6	3.1		V_{GS} = 4.5V, I_D = 72A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.2	1.7	2.2	V	V_{DS} = V_{GS}, I_D = 100μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	——	-7.0	——	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} =24 V, V_{GS} = 0V
		——	——	150		V_{DS} =24V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
gfs	Forward Transconductance	189	——	——	S	V_{DS} = 15V, I_D =72A
Q_g	Total Gate Charge	——	36	54	nC	V_{DS} = 15V V_{GS} = 4.5V I_D = 72A
Q_{gs1}	Pre-Vth Gate-to-Source Charge	——	10	——		
Q_{gs2}	Post-Vth Gate-to-Source Charge	——	7.7	——		
Q_{gd}	Gate-to-Drain Charge	——	10	——		
Q_{godr}	Gate Charge Overdrive	——	8.3	——		
Q_{sw}	Switch Charge (Qgs2 + Qgd)	——	20	——		
R_G	Gate Resistance	——	2.0	——	Ω	
$t_{d(on)}$	Turn-On Delay Time	——	19	——	ns	V_{DD} = 15V I_D = 72A R_G= 1.8Ω V_{GS} = 4.5V ④
t_r	Rise Time	——	98	——		
$t_{d(off)}$	Turn-Off Delay Time	——	28	——		
t_f	Fall Time	——	30	——		
C_{iss}	Input Capacitance	——	4945	——	pF	V_{GS} = 0V V_{DS} = 15V f = 1.0MHz
C_{oss}	Output Capacitance	——	908	——		
C_{rss}	Reverse Transfer Capacitance	——	493	——		

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	180	mJ
$E_{AS\ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑥	279	
I_A	Avalanche Current	72	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ②	——	——	179①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	357		
V_{SD}	Diode Forward Voltage	——	——	1.0	V	T_J = 25°C,I_S = 72A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	31	47	ns	T_J = 25°C I_F = 72A ,V_{DD}=15V
Q_{rr}	Reverse Recovery Charge	——	87	130	nC	di/dt = 360A/μs ④

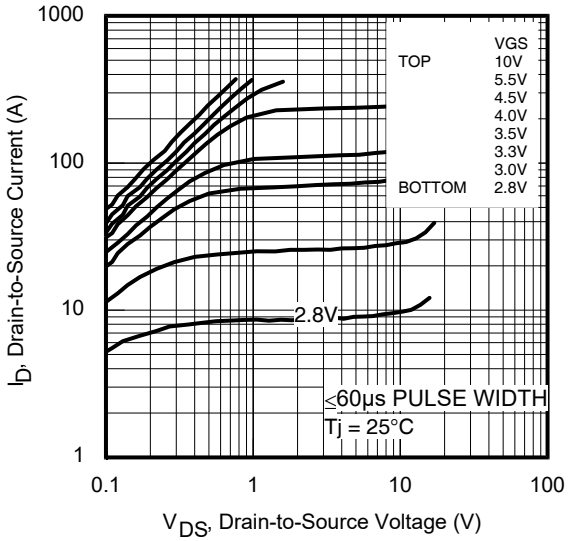


Fig 1. Typical Output Characteristics

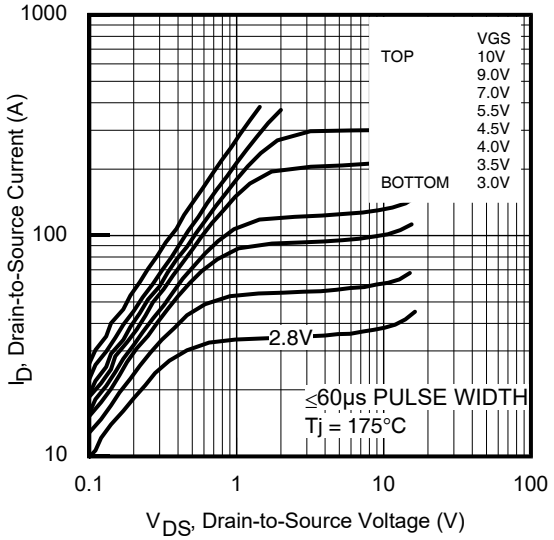


Fig 2. Typical Output Characteristics

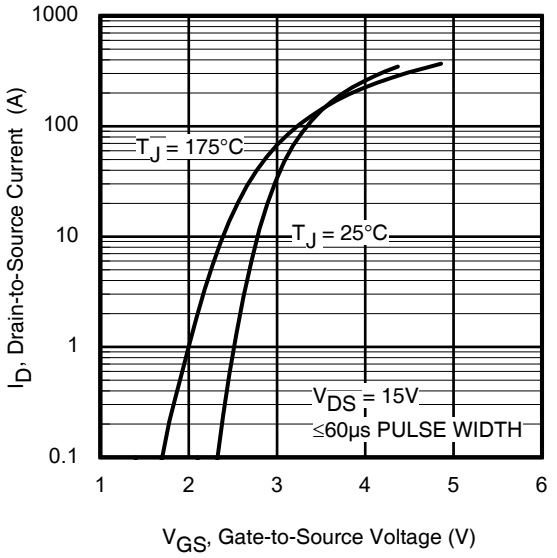


Fig 3. Typical Transfer Characteristics

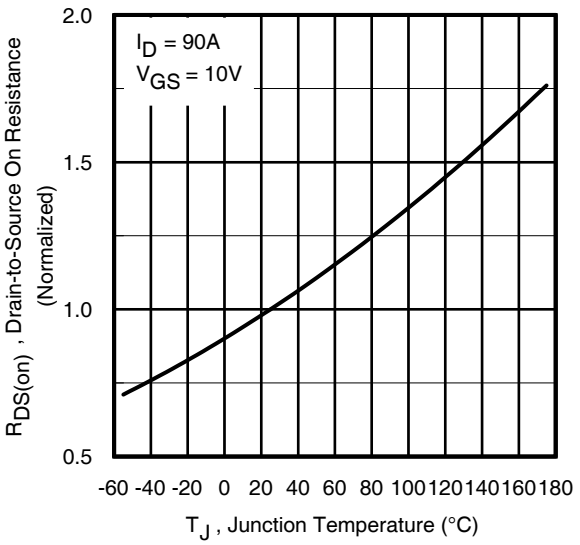


Fig 4. Normalized On-Resistance vs. Temperature

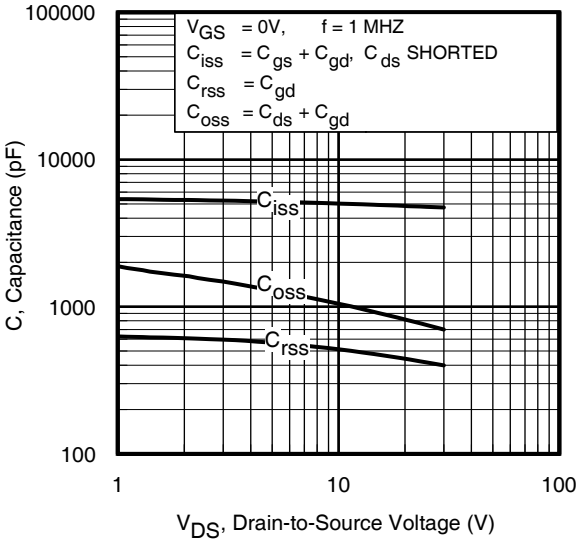


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

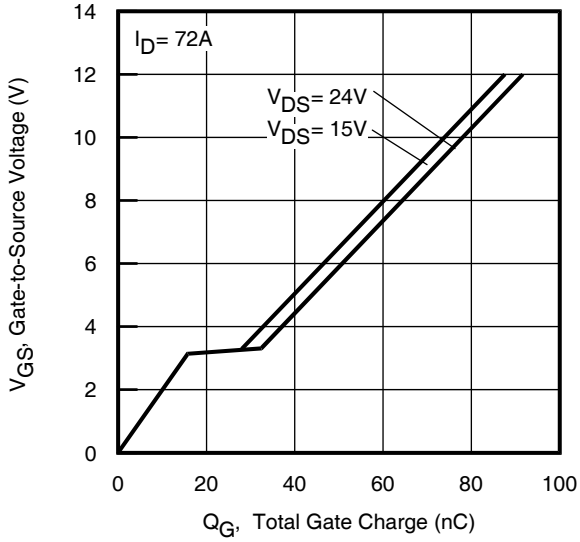


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

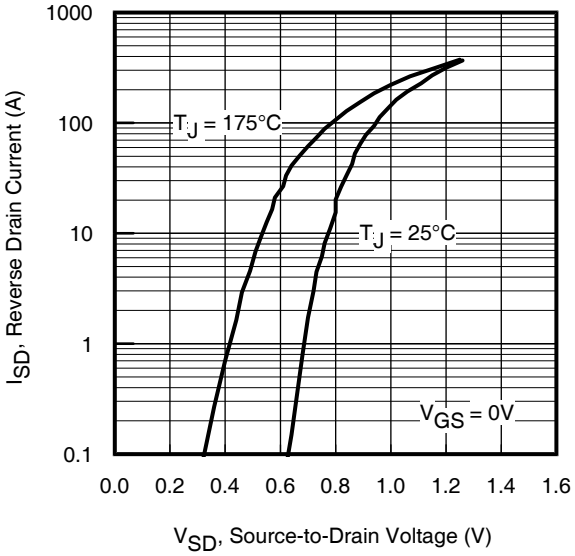


Fig 7. Typical Source-Drain Diode Forward Voltage

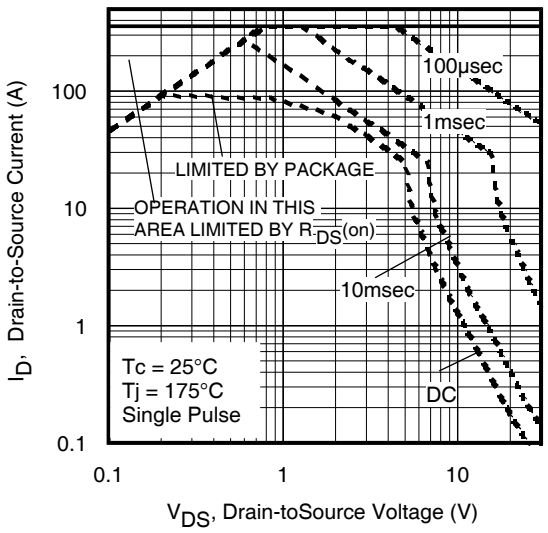


Fig 8. Maximum Safe Operating Area

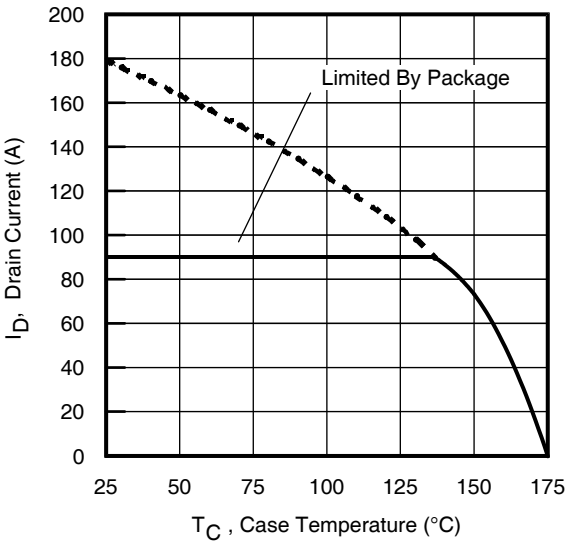


Fig 9. Maximum Drain Current vs. Case Temperature

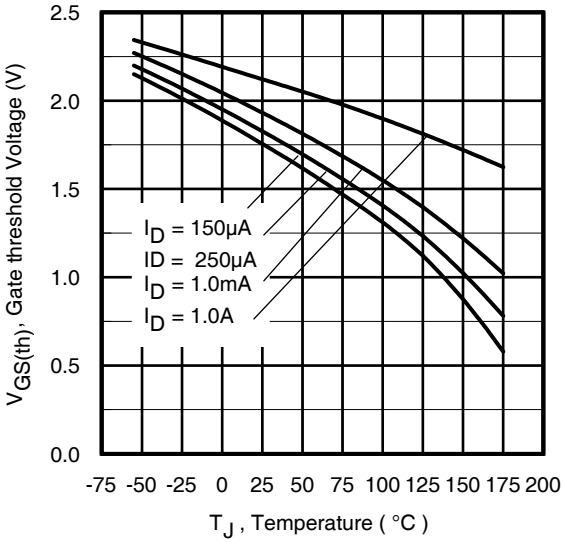


Fig 10. Threshold Voltage vs. Temperature

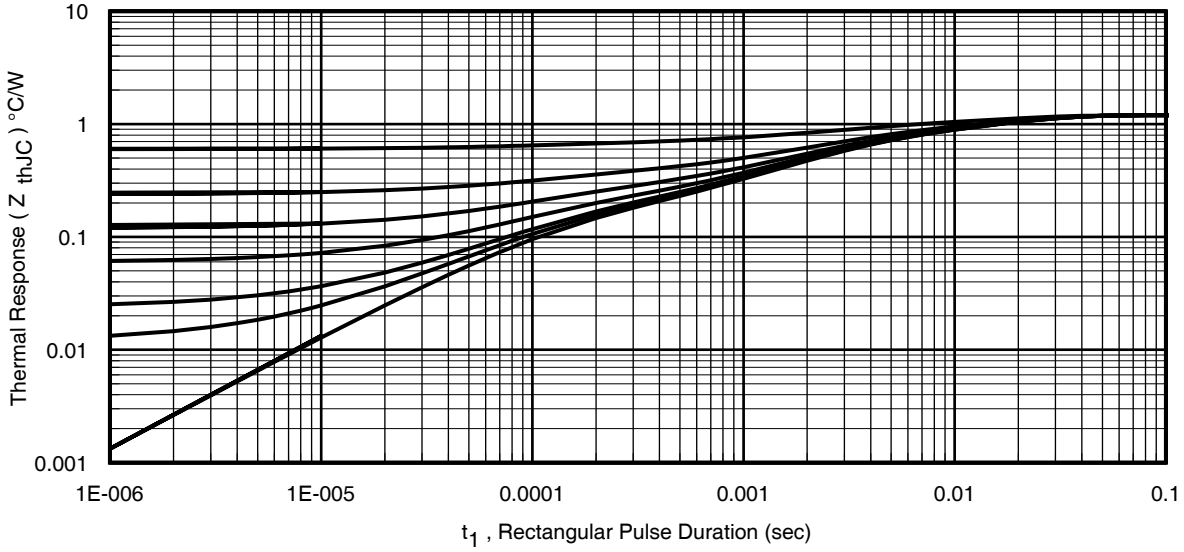


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

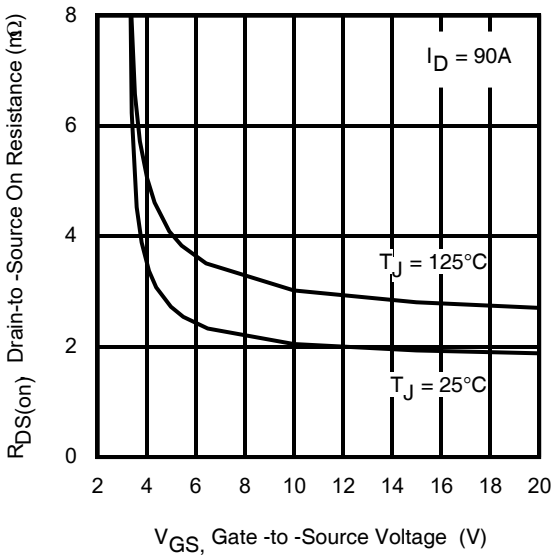


Fig 12. Typical On-Resistance vs. Gate Voltage

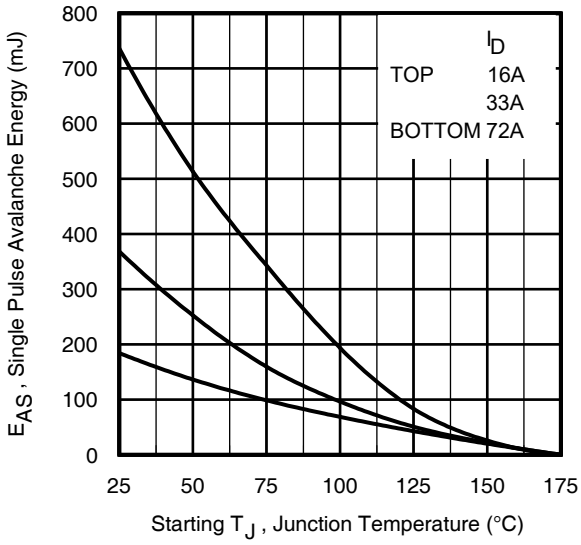


Fig 13. Maximum Avalanche Energy vs. Drain Current

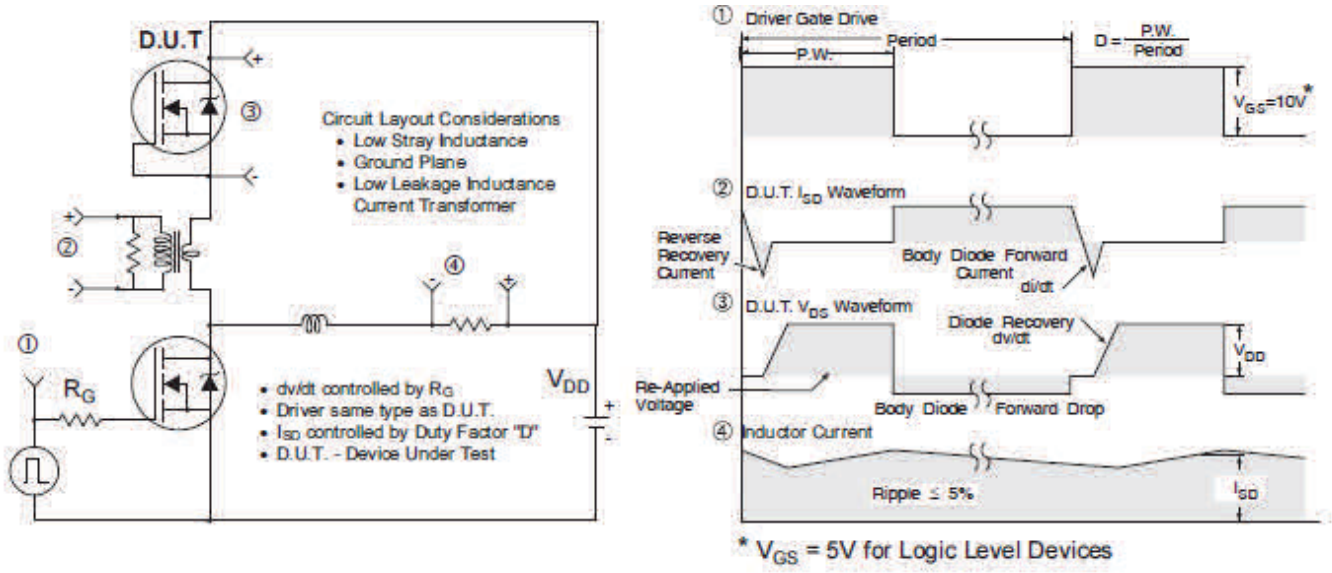


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel Power MOSFETs

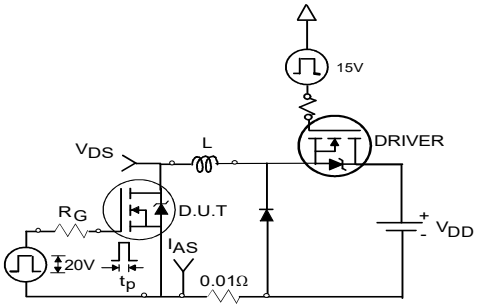


Fig 15a. Unclamped Inductive Test Circuit

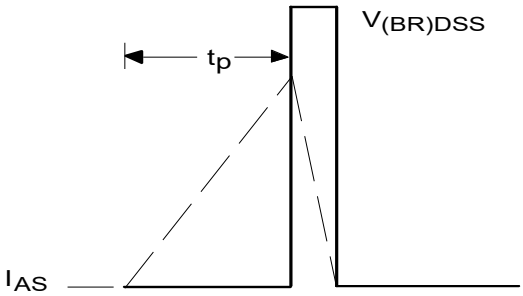


Fig 15b. Unclamped Inductive Waveforms

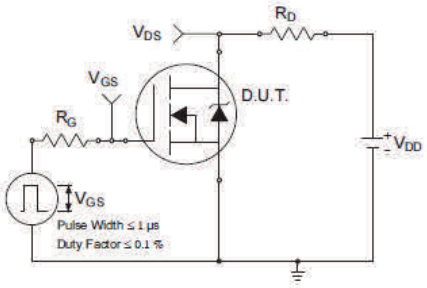


Fig 16a. Switching Time Test Circuit

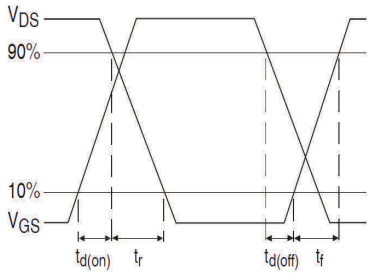


Fig 16b. Switching Time Waveforms

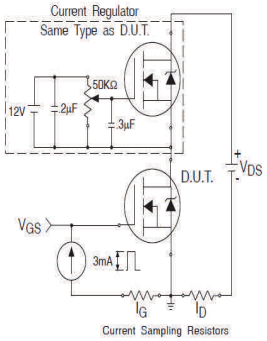


Fig 17a. Gate Charge Test Circuit

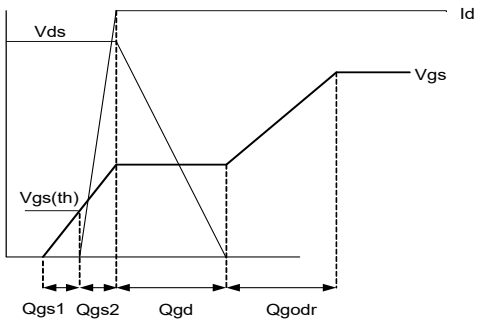


Fig 17b. Gate Charge Waveform