



Group-Semi N-Channel MOSFET

Dec 2016

GENERAL DESCRIPTION

GroupSemiconductor(GS) has series Trench power MOSFET platforms for voltage up 20V to 200 volts, both with design service and manufacturing capability, including cell, termination design and simulation.

The GS 40V 120A N-Channel Power MOSFET is a Low voltage P channel Trench power MOSFET sample with advanced technology to have better characteristics, such as fast switching time, low Ciss and Crss, low on resistance and excellent avalanche characteristics, making it especially suitable for applications which require superior power density and outstanding efficiency.

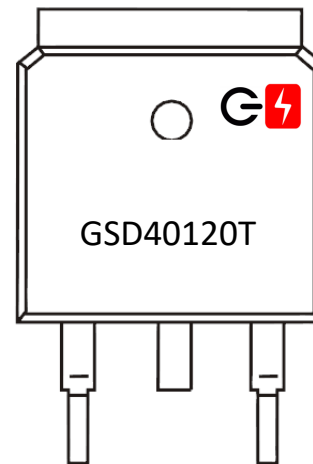
GENERAL FEATURES

- $V_{DS} = 40V, I_D = 120A$
 $R_{DS(ON)} < 4.2m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 6m\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- SR
- Inverters

Package	Pin Configuration (Top View)
TO-252	



Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BVDSS	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A, T_J = 25^\circ C$	40	-	-	V
V_{GS}	Gate-Source Voltage		± 25			V
I_D	Continuous Drain Current	$TC = 25^\circ C$ $TC = 100^\circ C$	120 80			A
I_{DM}	Pulsed Drain Current ^C		240			A
I_{AS}	Avalanche Current ^C		40			A
EAS	Avalanche energy $L = 0.1mH$ ^C		46			mJ
P_D	Power Dissipation ^B	$TC = 25^\circ C$ $TC = 100^\circ C$	83 33			W
P_{DSM}	Power Dissipation ^A	$TC = 25^\circ C$ $TC = 70^\circ C$	7.3 4.7			W
T_J, T_{STG}	Junction and Storage Temperature Range		-55 to 150			$^\circ C$
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 40V, V_{GS} = 0V$ $-T_J = 55^\circ C$	-	-	1 5	μA μA
IGSSF	Gate-Body Leakage Current, Forward	$V_{GS} = 20V, V_{DS} = 0V$	-	-	100	nA
IGSSR	Gate-Body Leakage Current, Reverse	$V_{GS} = -20V, V_{DS} = 0V$	-	-	-100	nA



Thermal Characteristics						
R _{θJA}	Maximum Junction-to-Ambient ^A		14			°C/W
	Maximum Junction-to-Ambient ^{AD}		40			°C/W
R _{θJC}	Maximum Junction-to-Case		1.1			°C/W
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.8	2.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 20A V _{GS} = 4.5V, I _D = 20A	-	4 5	4.5 6	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 5V, I _D = 20A	-	80	-	S
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	1.8	-	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 20V, V _{GS} = 0V, f=1MHz	-	1200	-	pF
C _{oss}	Output Capacitance		-	540	-	pF
C _{rss}	Reverse Transfer Capacitance		-	52	-	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DS} = 20V, R _G = 3Ω, I _D = 20A , V _{GS} = 10V (Note 5, 6)	-	6.4	-	ns
t _r	Turn-On Rise Time		-	17	-	ns
t _{d(off)}	Turn-Off Delay Time		-	29	-	ns
t _f	Turn-Off Fall Time		-	16.8	-	ns
Q _g (10V)	Total Gate Charge	V _{DS} = 20V, I _D = 20A, V _{GS} =0~10V (Note 5, 6)	-	28	-	nC
Q _g (4.5V)	Total Gate Charge		-	23	-	nC
Q _{gs}	Gate-Source Charge		-	4.5	-	nC
Q _{gd}	Gate-Drain Charge		-	6.4	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		-	-	30	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	80	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 1A	-	0.7	1.2	V
t _{rr}	Reverse Recovery Time	I _F =20A, dI/dt=100A/us	-	30	-	ns
Q _{rr}	Reverse Recovery Charge		-	24	-	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

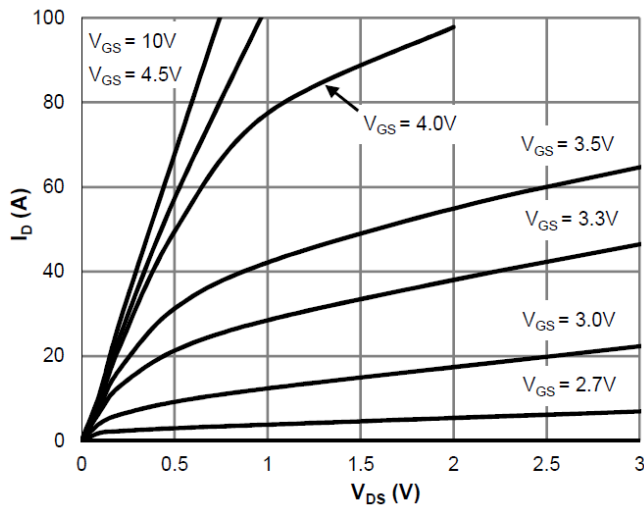


Figure 1: Saturation Characteristics

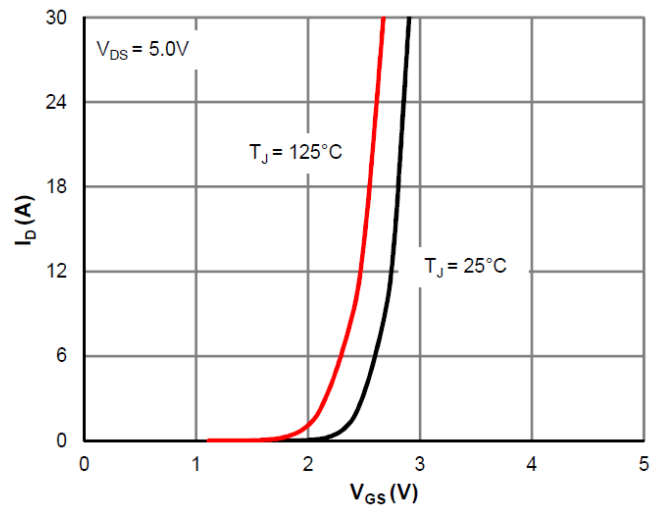


Figure 2: Transfer Characteristics

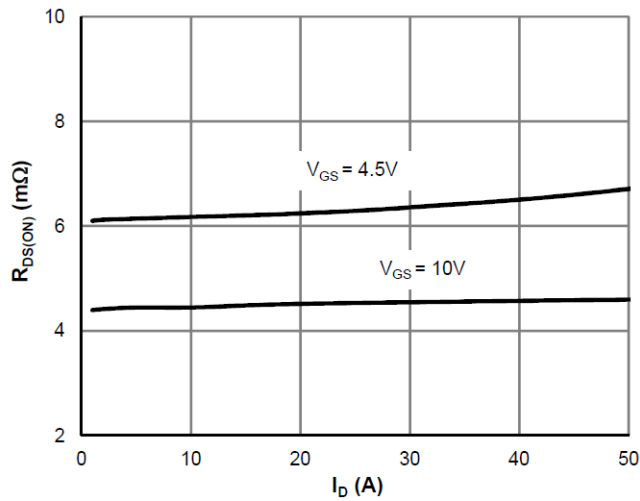


Figure 3: $R_{DS(ON)}$ vs. Drain Current

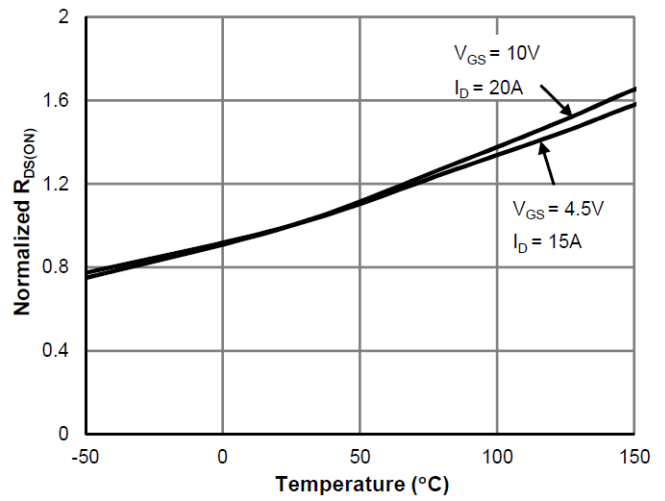


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

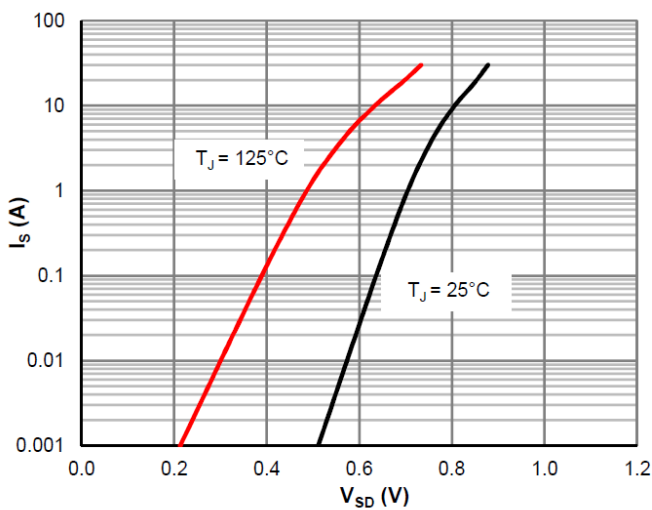


Figure 5: Body-Diode Characteristics

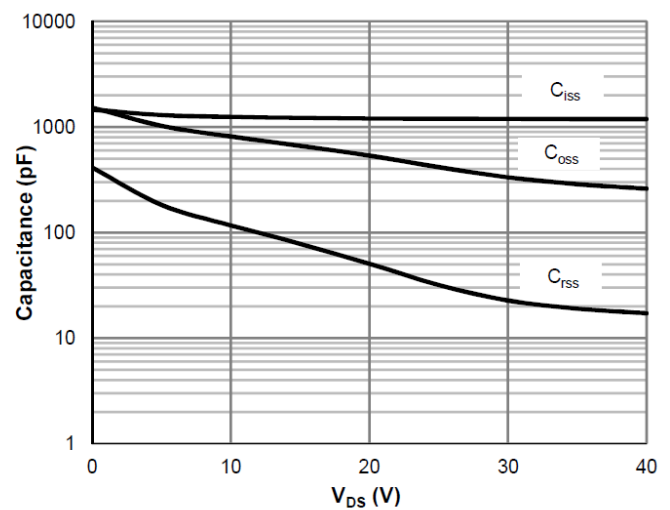


Figure 6: Capacitance Characteristics



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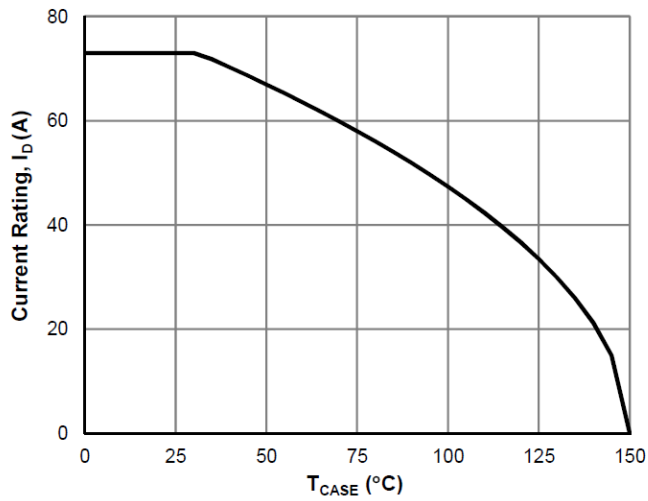


Figure 7: Current De-rating

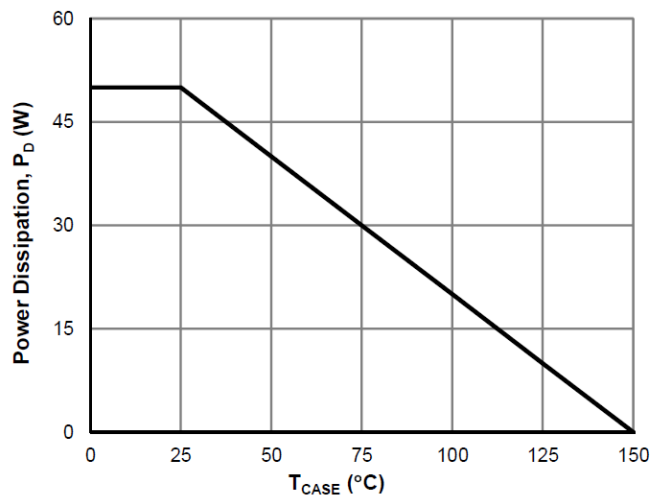


Figure 8: Power De-rating

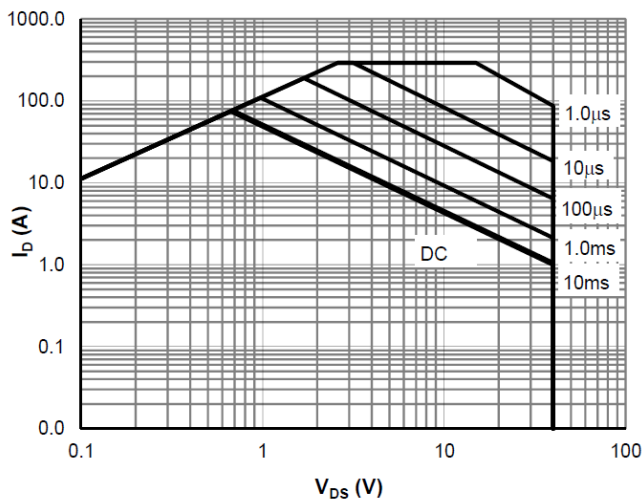


Figure 9: Safe operating area

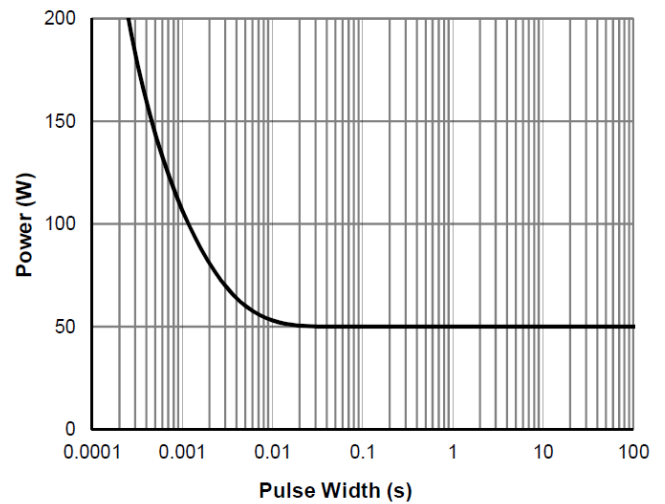


Figure 10: Single Pulse Power Rating, Junction-to-Case

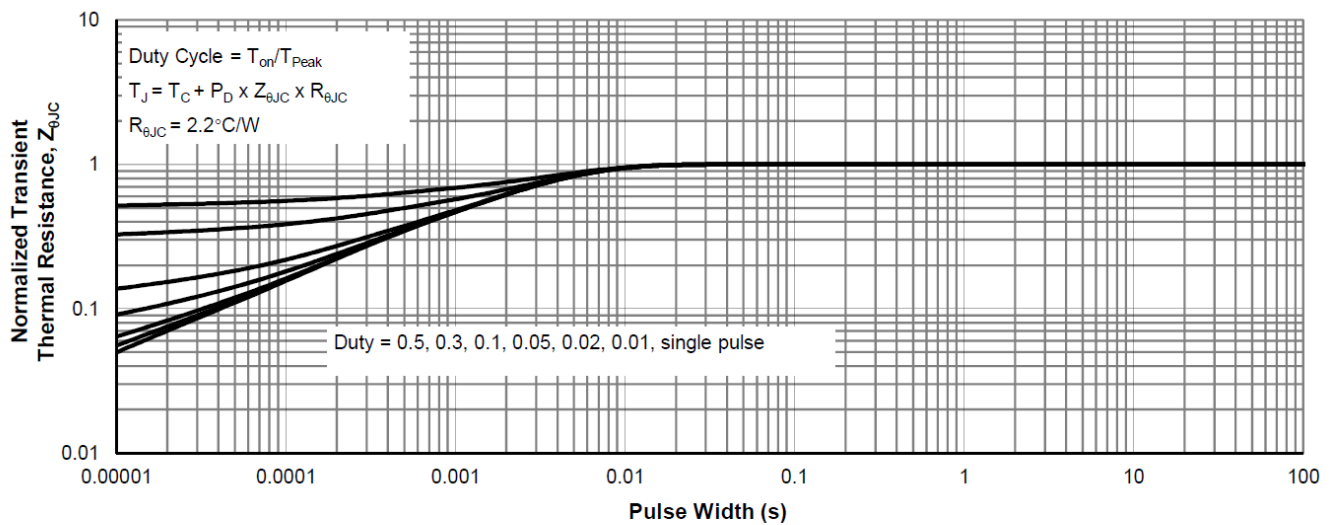
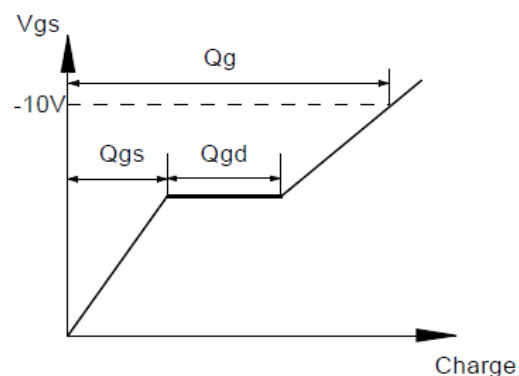
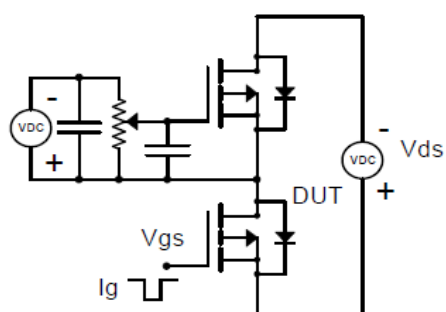


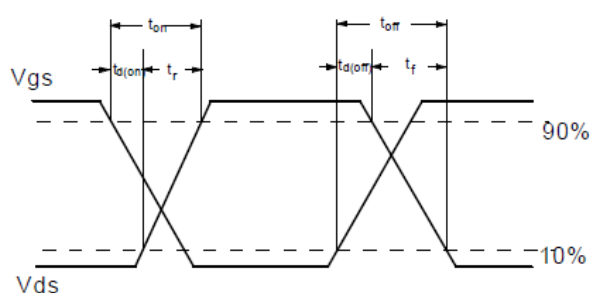
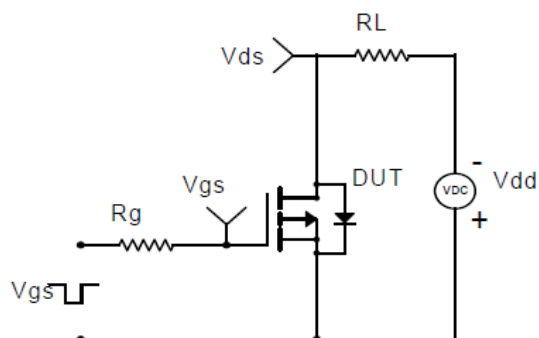
Figure 11: Normalized Maximum Transient Thermal Impedance

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

