GSD3040T N-Channel MOSFET

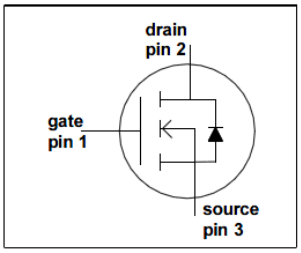
Group-Semi N-Channel MOSFET

Dec 2020

GENERAL DESCRIPTION

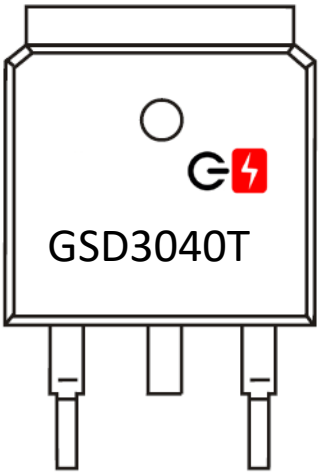
Group Semiconductor (GS) has series Trench power MOSFET platforms for voltage up 20V to 200 volts, both with design service and manufacturing capability, including cell, termination design and simulation.

The GS 30V 40A N-Channel Power MOSFET is a Low voltage P channel Trench power MOSFET sample with advanced technology to have better characteristics, such as fast switching time, low Ciss and Crss, low on resistance and excellent avalanche characteristics, making it especially suitable for applications which require superior power density and outstanding efficiency.

Package	Pin Configuration (Top View)
TO-252	

GENERAL FEATURES

- VDS =30V,ID =20A
  DS(ON) <10mΩ @ VGS=10V
  RDS(ON) <12mΩ @ VGS=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability



Application

- SR
- Inverters

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BVDSS	Drain-Source Breakdown Voltage	VGS = 0V, ID = 250μA, TJ = 25℃	30	-	-	V
V_{gs}	Gate-Source Voltage		±20			V
I_D	Continuous DrainCurrent	TC=25°C TC=100°C	40 28			A
I_{DM}	Pulsed Drain Current [C]		130			A
I_{AS}	Avalanche Current [C]		15			A
E_{AS}	Avalanche energy L=0.1mH [C]		100			mJ
P_D	Power Dissipation [B]	TC=25°C TC=70°C	3.1 2			W
T_J, T_{STG}	Junction and Storage Temperature Range		-55 to 150			°C
IDSS	Zero Gate Voltage Drain Current	VDS = 60V, VGS = 0V -TJ = 55℃	-	- -	1 5	μA μA
IGSSF	Gate-Body Leakage Current, Forward	VGS = 12V, VDS = 0V	-	-	100	nA
IGSSR	Gate-Body Leakage Current, Reverse	VGS = -12V, VDS = 0V	-	-	-100	nA

Thermal Characteristics						
$R_{\theta JA}$	Maximum Junction-to-Ambient [A]		40			°C/W
	Maximum Junction-to-Ambient [A D]		75			°C/W
$R_{\theta JC}$	Maximum Junction-to-Case		24			°C/W
On Characteristics						
VGS(th)	Gate Threshold Voltage	VDS = VGS, ID = 250μA	0.6	0.8	1	V
RDS(on)	Static Drain-Source On-Resistance	VGS = 10V, ID = 20A VGS = 4.5V, ID =18A	-	4.5 5	5.5 7	mΩ
gFS	Forward Transconductance	VDS = 4.5V, ID = 20A	-	70	-	S
Rg	Gate resistance	VGS=0V, VDS=0V, f=1MHz	-	3.2	-	Ω
Dynamic Characteristics						
Ciss	Input Capacitance	VDS = 15V, VGS = 0V, f=1MHz	-	1150	-	pF
Coss	Output Capacitance		-	180	-	pF
Crss	Reverse Transfer Capacitance		-	105	-	pF
Switching Characteristics						
td(on)	Turn-On Delay Time	VDS = 15V, RG = 3Ω, ID = 20A , VGS = 10V (Note 5, 6)	-	6.5	-	ns
tr	Turn-On Rise Time		-	2	-	ns
td(off)	Turn-Off Delay Time		-	17	-	ns
tf	Turn-Off Fall Time		-	3.5	-	ns
Qg(10V)	Total Gate Charge	VDS = 15V, ID = 20A,	-	20	-	nC
Qg(4.5V)	Total Gate Charge		-	9.5	-	nC
Qgs	Gate-Source Charge		-	2.7	-	nC
Qgd	Gate-Drain Charge		-	5	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
IS	Maximum Continuous Drain-Source Diode Forward Current		-	-33	-	A
ISM	Maximum Pulsed Drain-Source Diode Forward Current		-	-	-	A
VSD	Drain-Source Diode Forward Voltage	VGS = 0V, IS = 1A	-	0.7	1.2	V
trr	Reverse Recovery Time	IF=30A, dI/dt=100A/us	-	8.7	-	ns
Qrr	Reverse Recovery Charge		-	13.5	-	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

G. The maximum current limited by package.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

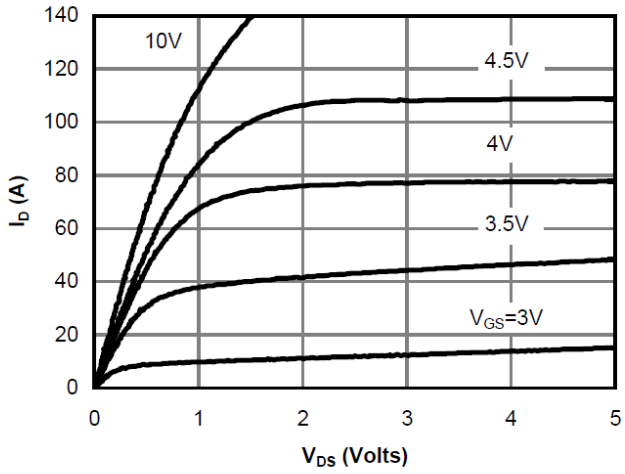


Fig 1: On-Region Characteristics (Note E)

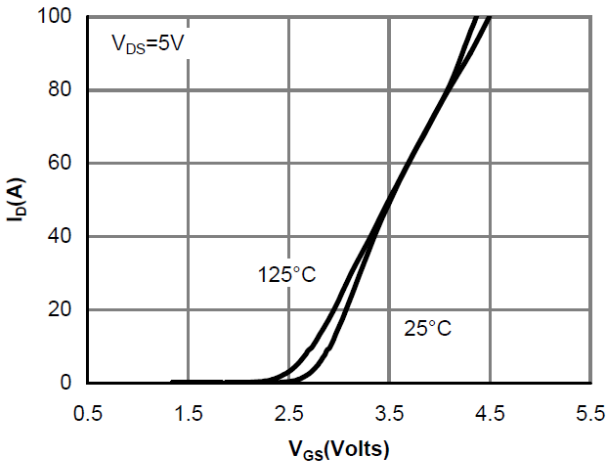


Figure 2: Transfer Characteristics (Note E)

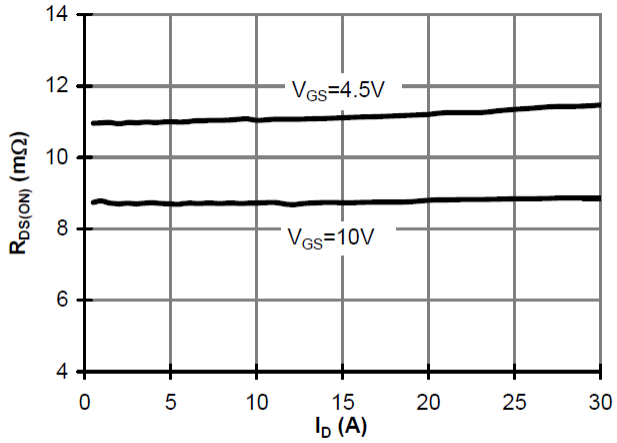


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

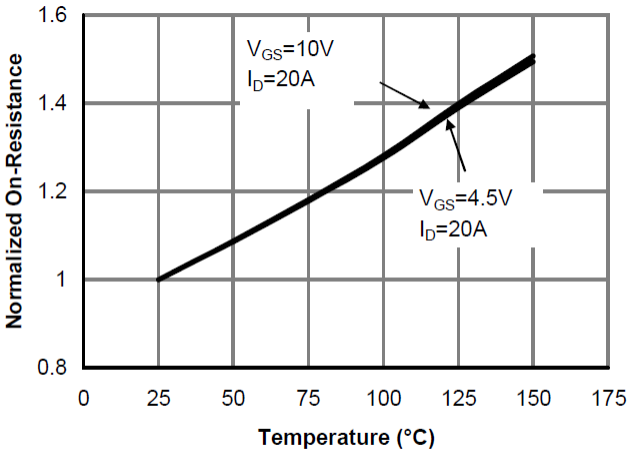


Figure 4: On-Resistance vs. Junction Temperature (Note E)

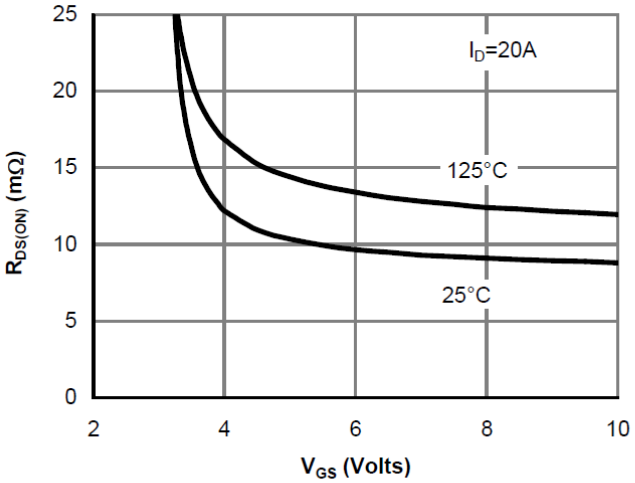


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

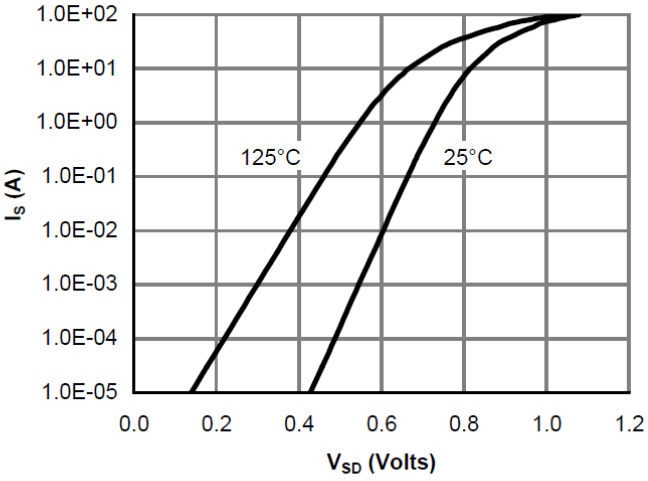


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

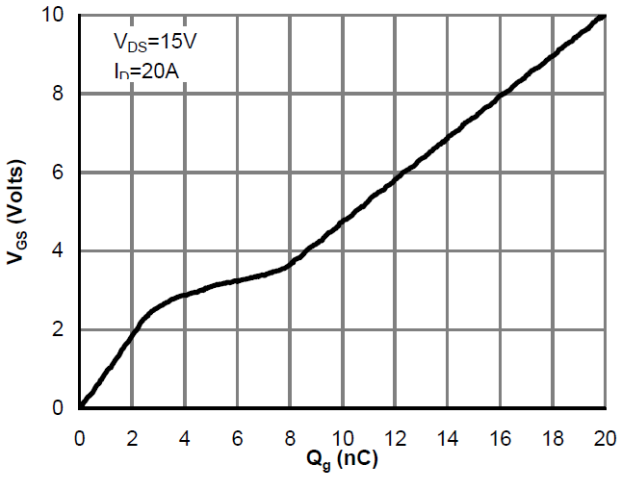


Figure 7: Gate-Charge Characteristics

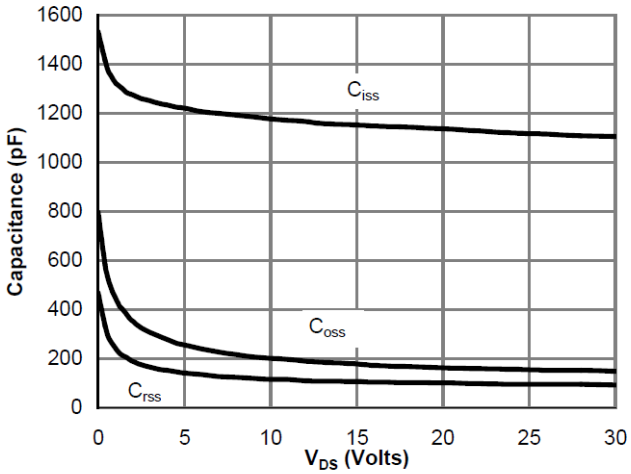


Figure 8: Capacitance Characteristics

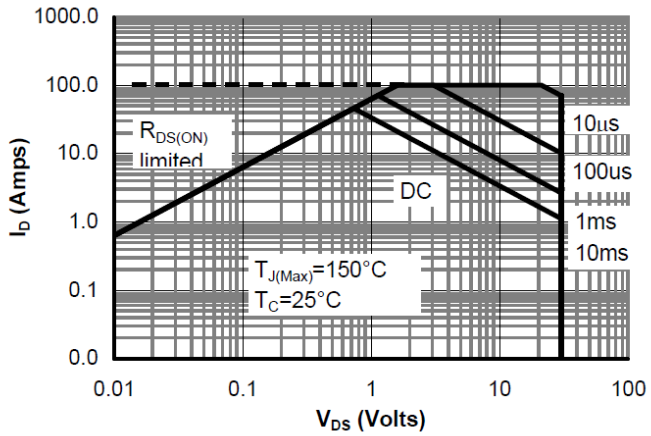


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

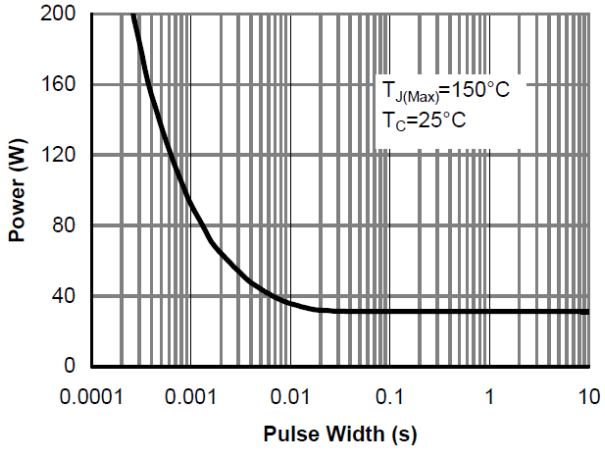


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

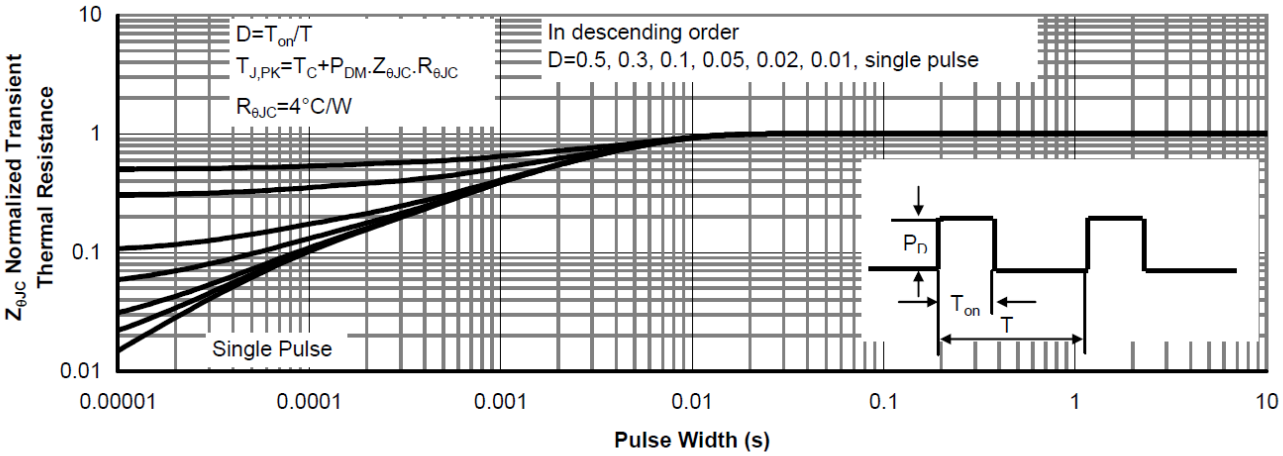


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

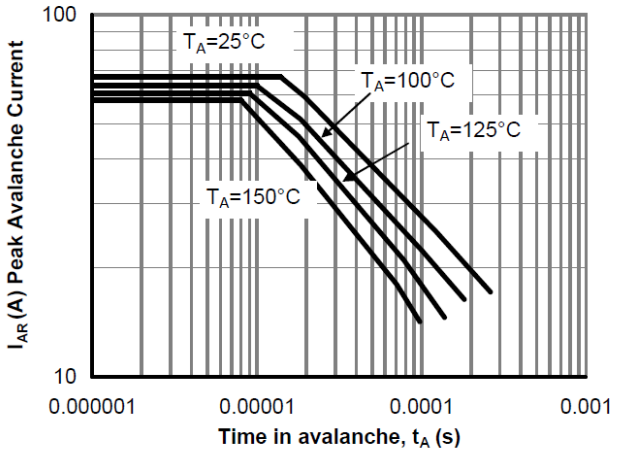


Figure 12: Single Pulse Avalanche capability (Note C)

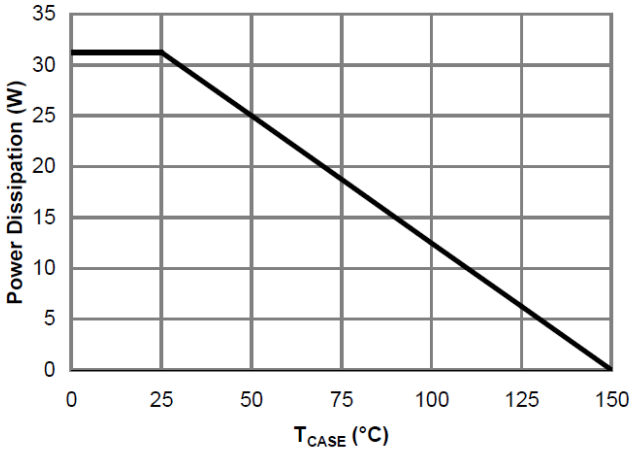


Figure 13: Power De-rating (Note F)

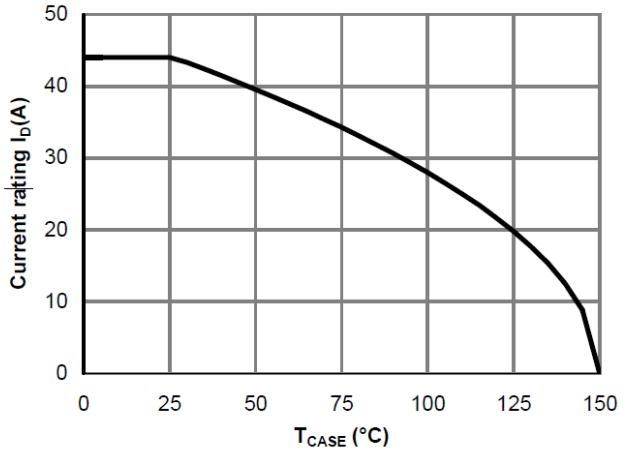


Figure 14: Current De-rating (Note F)

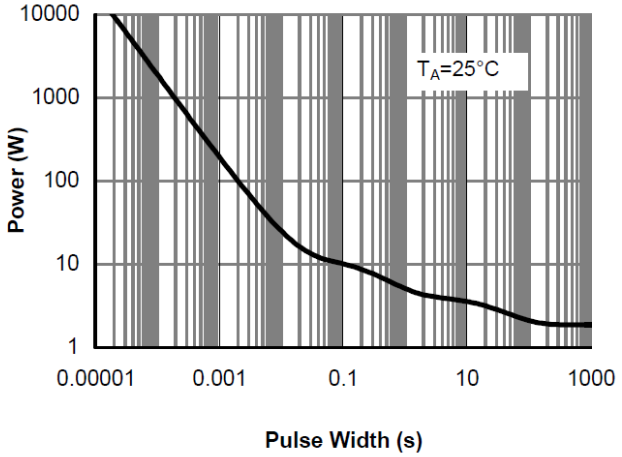


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

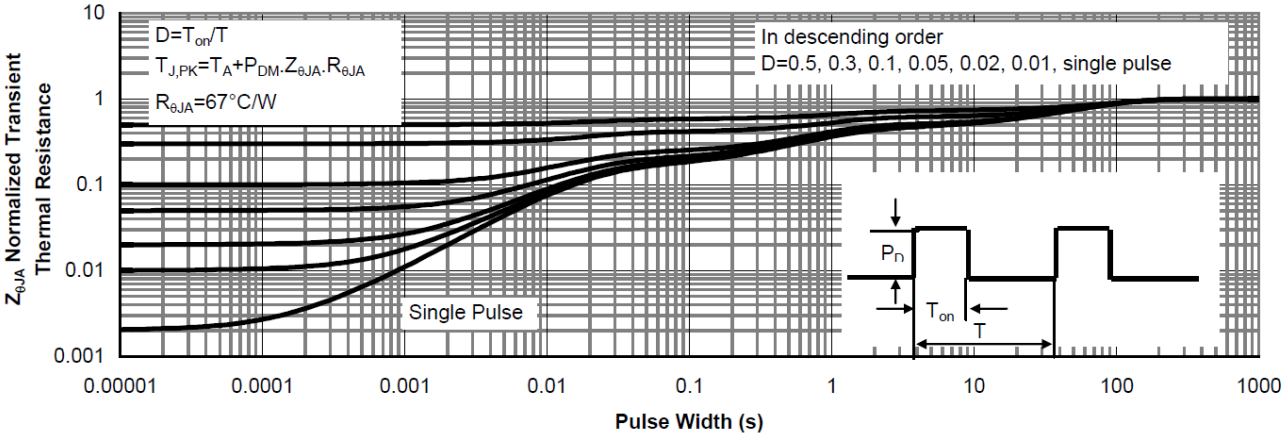
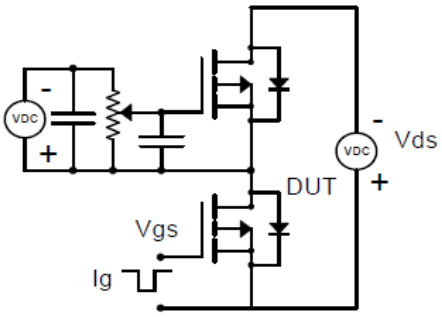
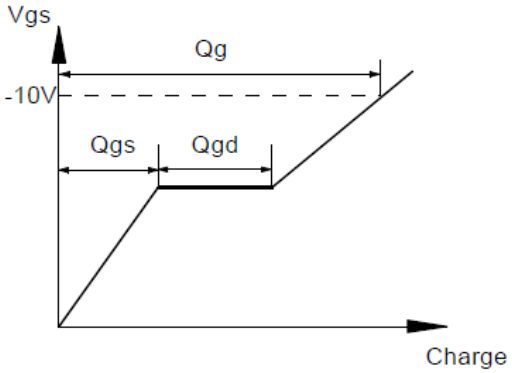


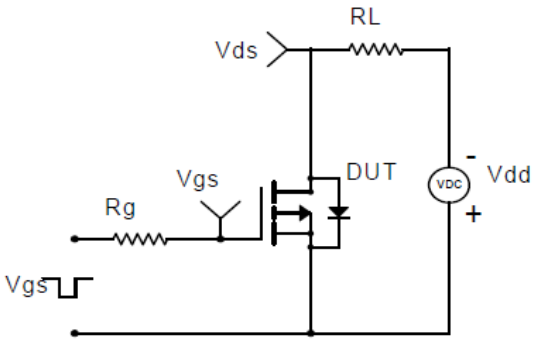
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

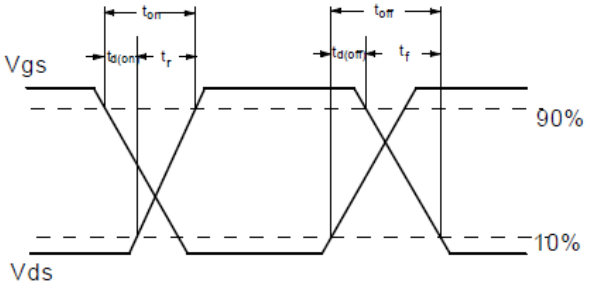
Gate Charge Test Circuit & Waveform





Resistive Switching Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms