



GSX18N60E

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

Super Junction MOSFET

600V Super Junction Power Transistor

GSX18N60E

Data Sheet

Ver 1.1

2019-3-20

600V 18A Power MOSFET

■ Description

GroupSemiconductor(GS) has series Multi-EPI Super-Junction power MOSFET platforms for voltage up 500V to 1000 volts, both with design service and manufacturing capability, including cell, termination design and simulation.

The GS 600V 18A Power MOSFET is a Low voltage N channel Multi-EPI Super-Junction power MOSFET sample with advanced technology to have better characteristics, such as fast switching time, low Ciss and Crss, low on resistance and excellent avalanche characteristics, making it especially suitable for applications which require superior power density and outstanding efficiency.

■ Features

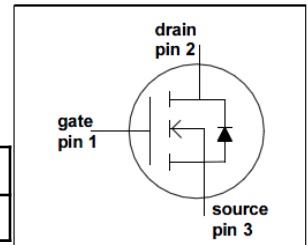
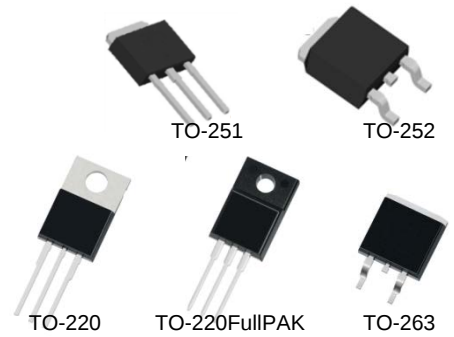
$R_{DS(ON)} = 0.25\Omega$ @ $V_{GS} = 10V$

$V_{DS} = 600V$

I_D (@ $V_{GS} = 10V$) = 9A

■ PKG

DFN8*8



GSA18N60E	GSP18N60E	GSB18N60E	GSD18N60E	GSS18N60E	GSL18N60E
TO-220Fullpak	TO-220	TO-263	TO-252	TO-251	DFN8*8

■ Absolute Maximum Ratings (TC = 25° C, unless otherwise specified)

Symbol	Parameter	GSP18N60E	GSA18N60E	Unit
V_{DS}	Drain-Source Voltage	600		V
I_D	Drain Current -Continuous (TC = 25°C) -Continuous (TC = 100°C)	18* 13*		A
I_{DM}	Drain Current - Pulsed (Note 1)	55		A
V_{GS}	Gate-Source voltage	±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	320		mJ
I_{AR}	Avalanche Current (Note 1)	3		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	2		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	15		V/ns
dV_{ds}/dt	Drain Source voltage slope (Vds=480V)	50		V/ns
P_D	Power Dissipation (TC = 25°C)	151	35	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		°C
T_L	Max. Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		°C

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■ Thermal Characteristics

Symbol	Parameter	GSA18N60E	GSP18N60E	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.2	1.2	$^{\circ}\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	0.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	62	$^{\circ}\text{C}/\text{W}$

Symbol	Parameter	Value (TO220)	Unit
$R_{\theta JA}^{(6)}$	Maximum Junction-to-Ambient	82	$^{\circ}\text{C}/\text{W}$
$R_{\theta CS}^{(6)}$	Maximum Case-to-sink	0.6	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}^{(7),(8)}$	Maximum Junction-to-Case θ	4.1	$\square^{\circ}\text{C}/\text{W}$

1. The power dissipation PD is based on $T_J(\text{MAX})=150^{\circ}\text{C}$ in a TO251 package, using junction-to-case thermal resistance.
2. Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^{\circ}\text{C}$.
3. $L=1\text{mH}$, Starting $T_J=25^{\circ}\text{C}$.
4. $L=10\text{mH}$, starting $T_J=25^{\circ}\text{C}$.
5. $L=60\text{mH}$, starting $T_J=25^{\circ}\text{C}$.
6. The tests are performed with the device with $T_A=25^{\circ}\text{C}$.
7. The $R_{\square JA}$ is the sum of the thermal impedance from junction to case $R_{\square JC}$ and case to ambient.
8. These curves are based on the junction-to-case thermal impedance, assuming a maximum junction temperature of $T_J(\text{MAX})=150^{\circ}\text{C}$.

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■ Electrical Characteristics (T_J=25° C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA, T _J = 25°C	600	--	--	V
		V _{GS} = 0V, I _D = 250μA, T _J = 150°C	--	650	--	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	--	0.6	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600V, V _{GS} = 0V -T _J = 150°C	--	-- 10	1 -	μA μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30V, V _{DS} = 0V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.5	--	4.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 9A	--	0.22	0.25	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40V, I _D = 9A	--	16	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	--	1230	-	pF
C _{oss}	Output Capacitance		--	30	-	pF
C _{rss}	Reverse Transfer Capacitance		--	2.6	--	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 400V, I _D =9A R _G = 20Ω (Note 4)	--	20	--	ns
t _r	Turn-On Rise Time		--	17	--	ns
t _{d(off)}	Turn-Off Delay Time		--	170	--	ns
t _f	Turn-Off Fall Time		--	13	--	ns
Q _g	Total Gate Charge	V _{DS} = 400V, I _D = 9A V _{GS} = 10V (Note 4)	--	42	--	nC
Q _{gs}	Gate-Source Charge		--	6	--	nC
Q _{gd}	Gate-Drain Charge		--	29	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	18	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	42	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 9A	--	0.9	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 9A	--	380	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt =100A/μs	--	4.5	--	μC

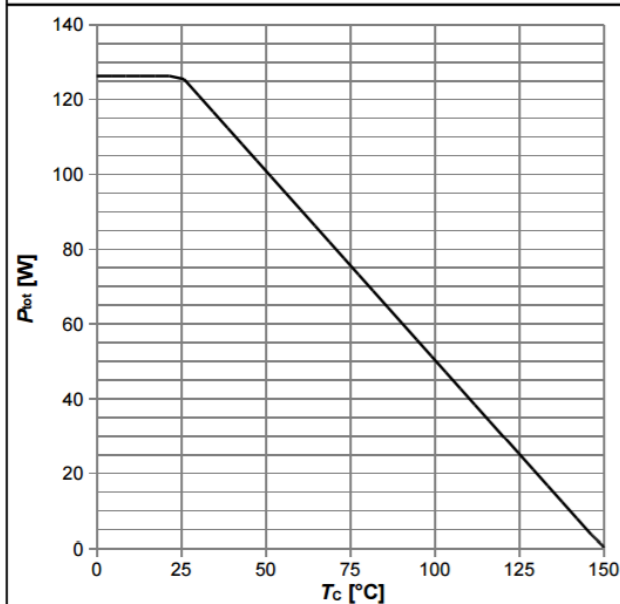
NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=60mH, I_{AS}=4A, V_{DD}=150V, Starting T_J=25 °C
3. I_{SD}≤4.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

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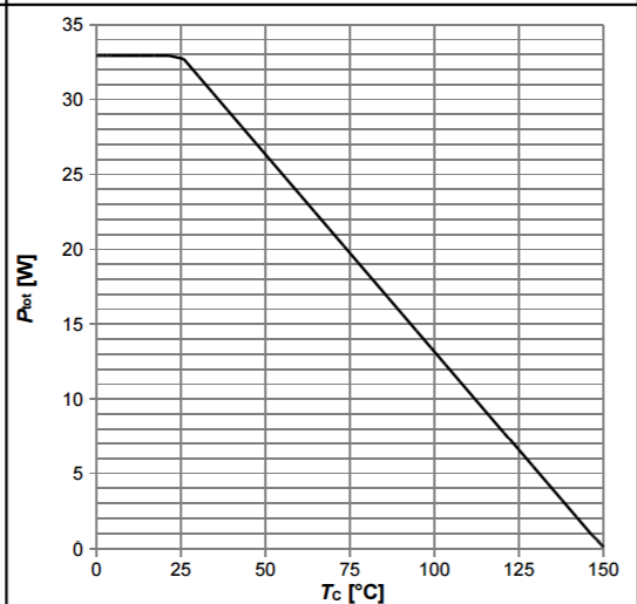
Typical Performance Characteristics

Diagram 1: Power dissipation (Non FullPAK)



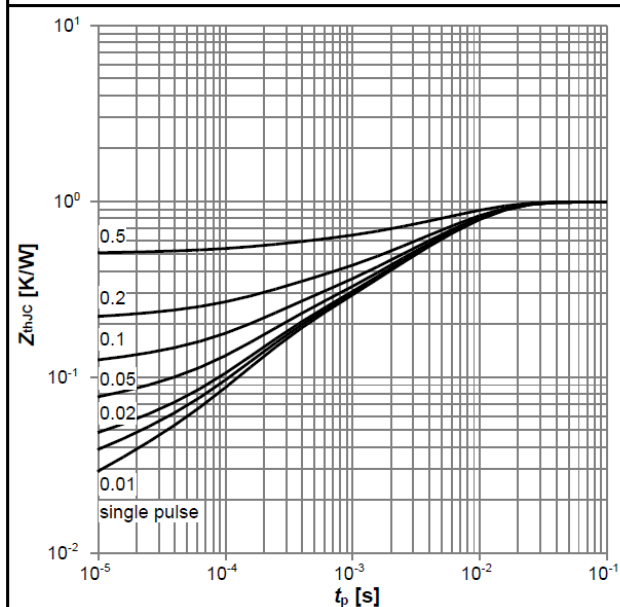
$$P_{tot}=f(T_c)$$

Diagram 2: Power dissipation (FullPAK)



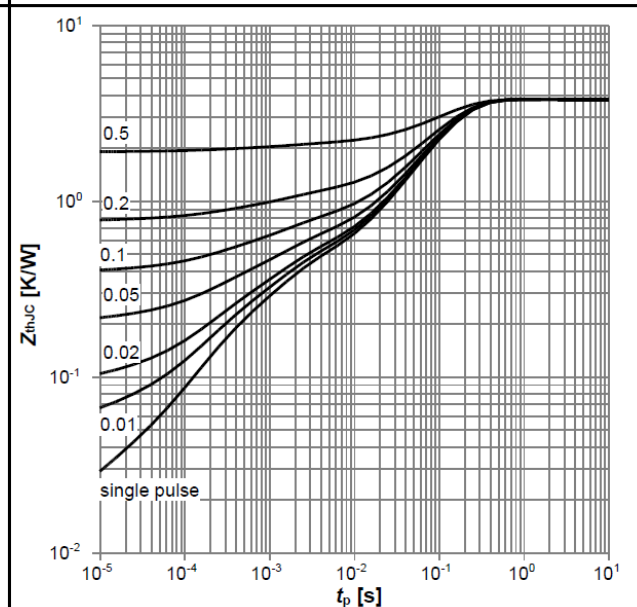
$$P_{tot}=f(T_c)$$

Diagram 3: Max. transient thermal impedance (Non FullPAK)



$$Z_{thJC}=f(t_p); \text{ parameter: } D=t_p/T$$

Diagram 4: Max. transient thermal impedance (FullPAK)

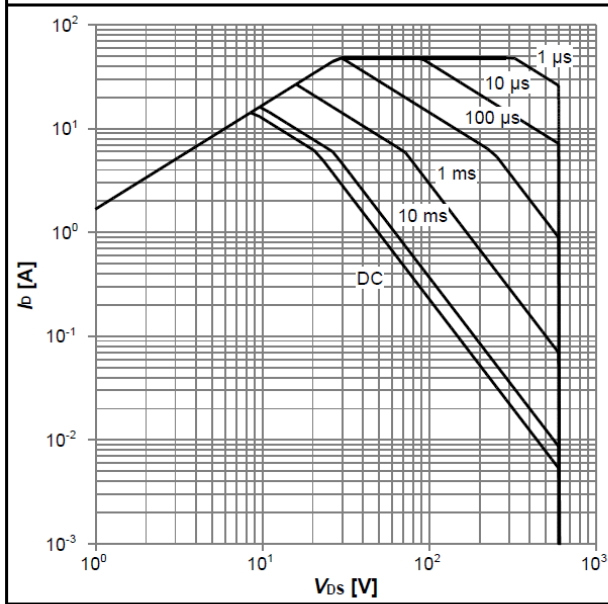


$$Z_{thJC}=f(t_p); \text{ parameter: } D=t_p/T$$

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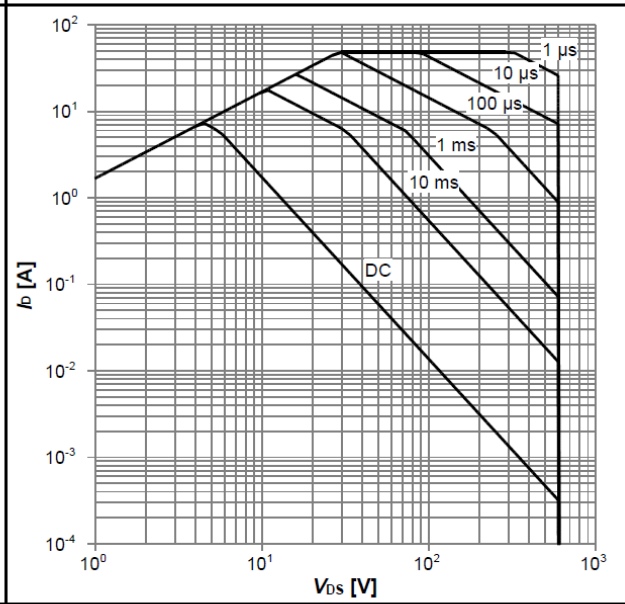
Typical Performance Characteristics

Diagram 5: Safe operating area (Non FullPAK)



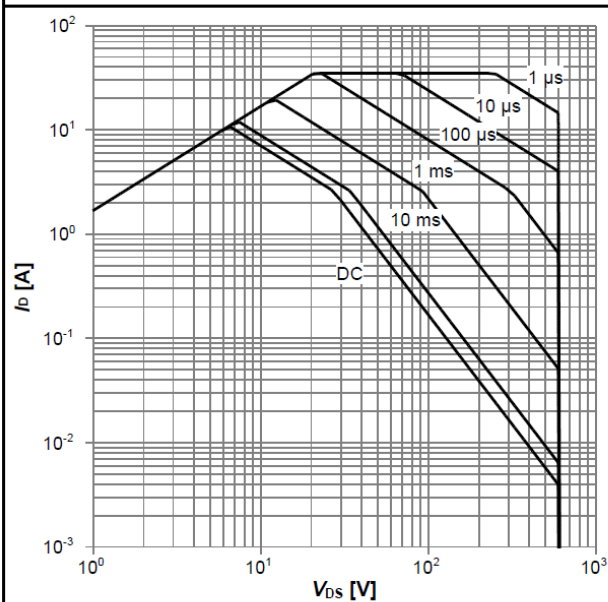
$I_D = f(V_{DS})$; $T_C = 25^\circ\text{C}$; $D = 0$; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



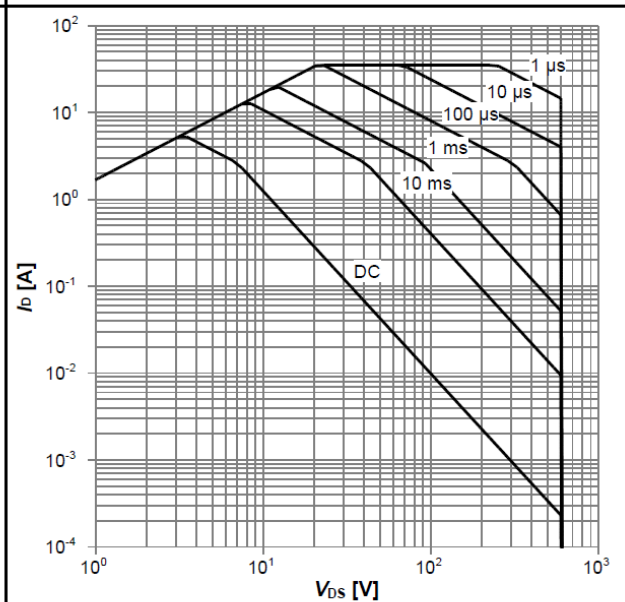
$I_D = f(V_{DS})$; $T_C = 25^\circ\text{C}$; $D = 0$; parameter: t_p

Diagram 7: Safe operating area (Non FullPAK)



$I_D = f(V_{DS})$; $T_C = 80^\circ\text{C}$; $D = 0$; parameter: t_p

Diagram 8: Safe operating area (FullPAK)

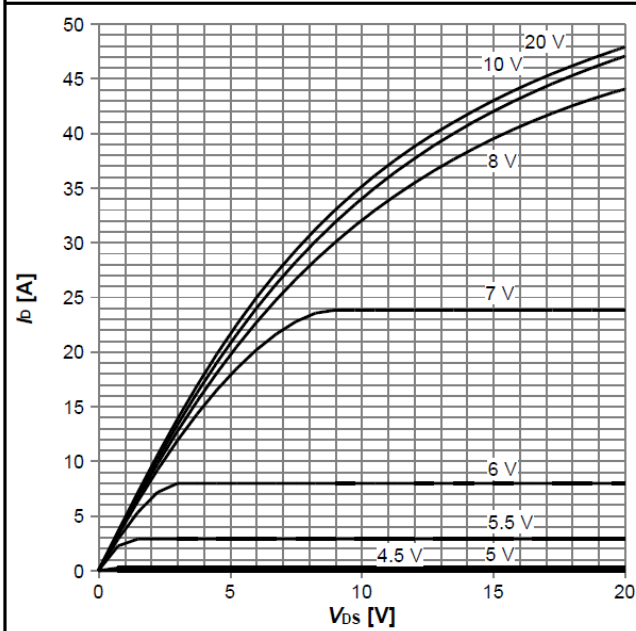


$I_D = f(V_{DS})$; $T_C = 80^\circ\text{C}$; $D = 0$; parameter: t_p

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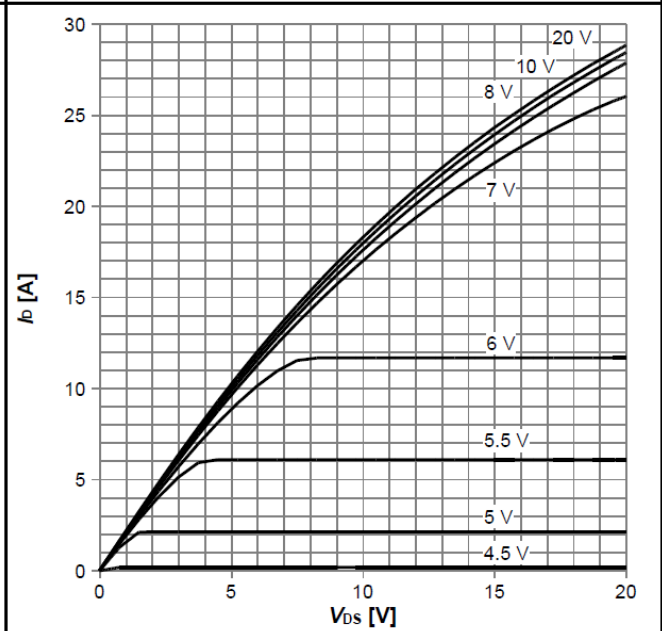
Typical Performance Characteristics

Diagram 9: Typ. output characteristics



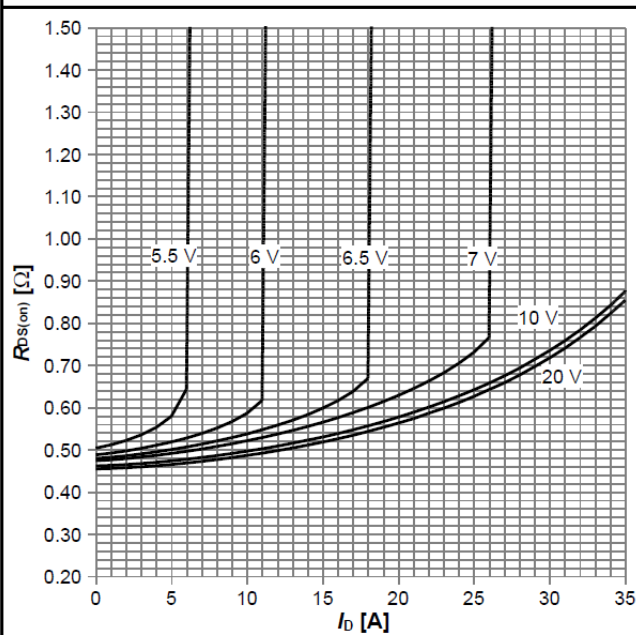
$I_D = f(V_{DS})$; $T_J = 25\text{ }^{\circ}\text{C}$; parameter: V_{GS}

Diagram 10: Typ. output characteristics



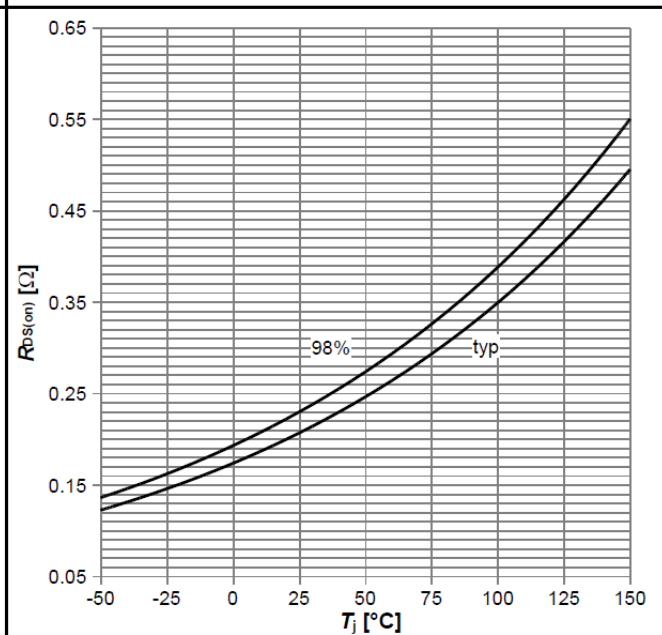
$I_D = f(V_{DS})$; $T_J = 125\text{ }^{\circ}\text{C}$; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D)$; $T_J = 125\text{ }^{\circ}\text{C}$; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance

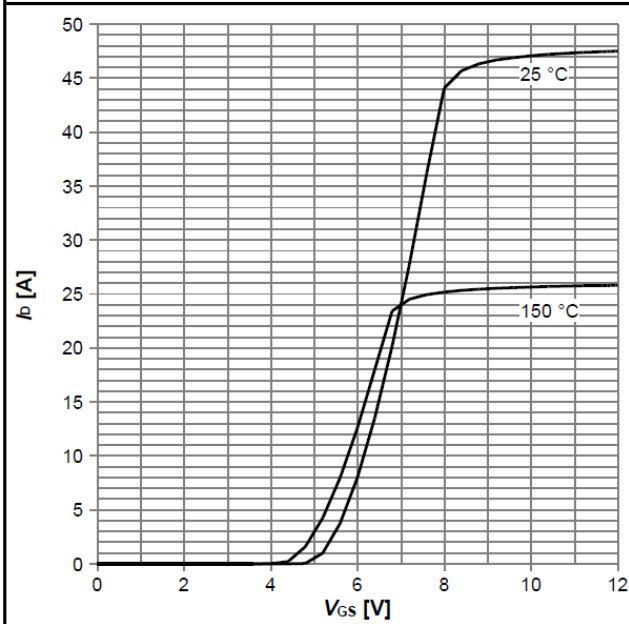


$R_{DS(on)} = f(T_J)$; $I_D = 6.4\text{ A}$; $V_{GS} = 10\text{ V}$

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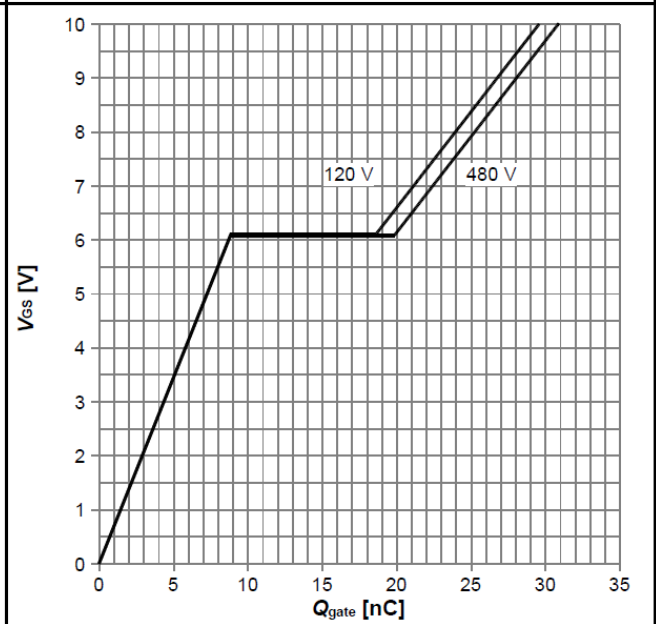
Typical Performance Characteristics

Diagram 13: Typ. transfer characteristics



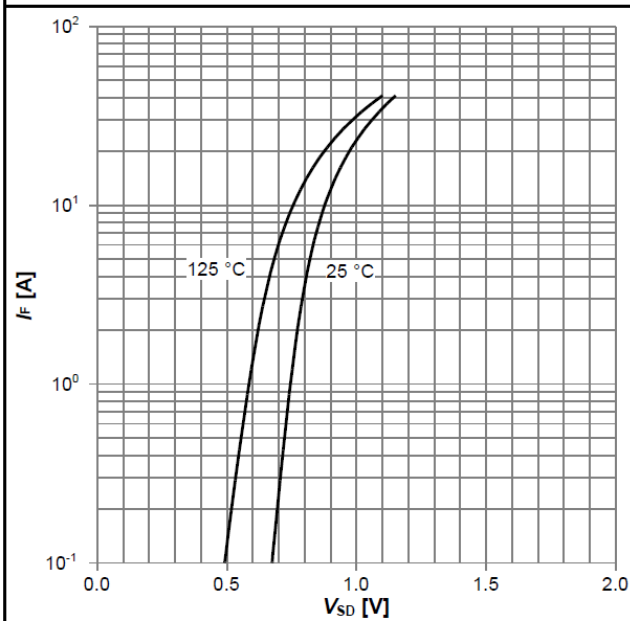
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 14: Typ. gate charge



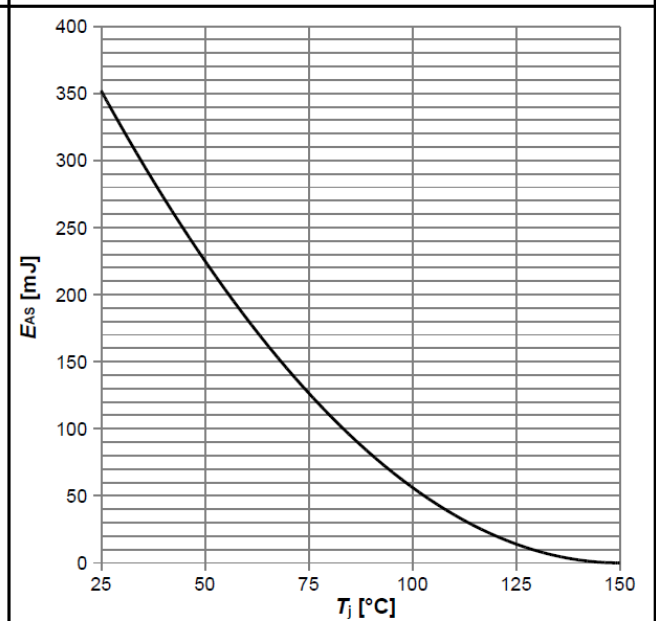
$V_{GS} = f(Q_{gate})$; $I_D = 8.0$ A pulsed; parameter: V_{DD}

Diagram 15: Forward characteristics of reverse diode



$I_F = f(V_{SD})$; parameter: T_j

Diagram 16: Avalanche energy

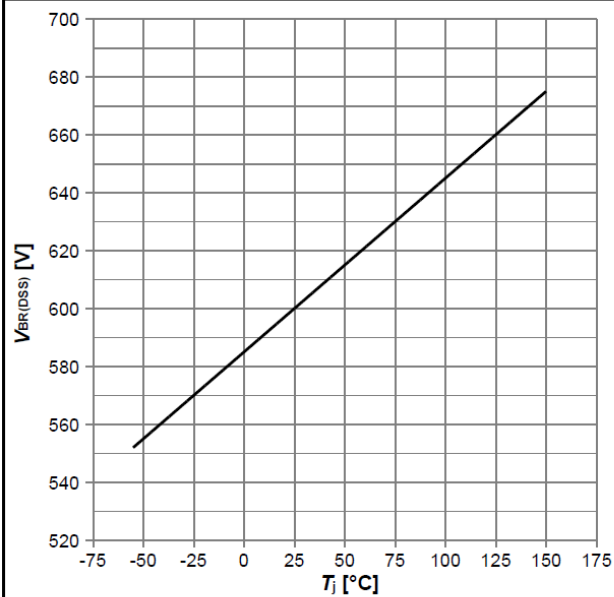


$E_{AS} = f(T_j)$; $I_D = 2.9$ A; $V_{DD} = 50$ V

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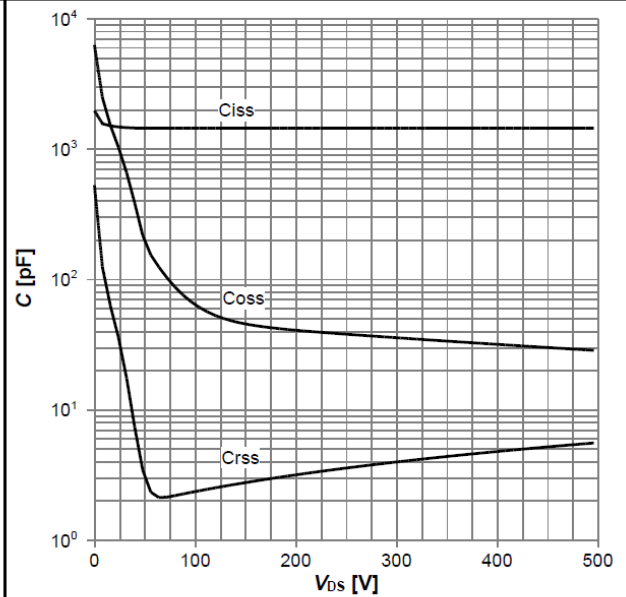
Typical Performance Characteristics

Diagram 17: Drain-source breakdown voltage



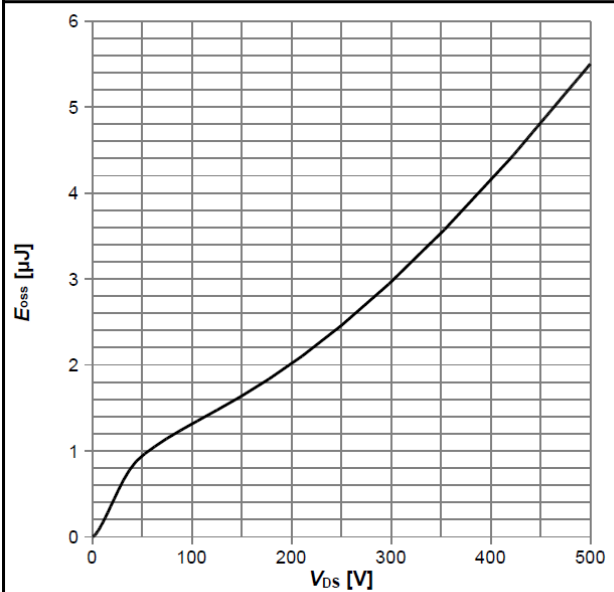
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 18: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 19: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

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Table 20 Switching times test circuit and waveform for inductive load

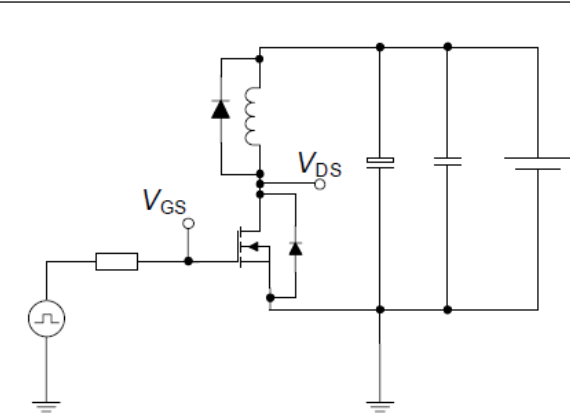
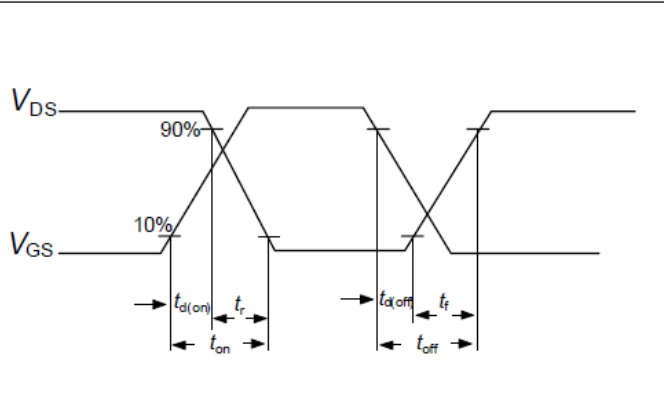
Switching times test circuit for inductive load	Switching time waveform
	

Table 21 Unclamped inductive load test circuit and waveform

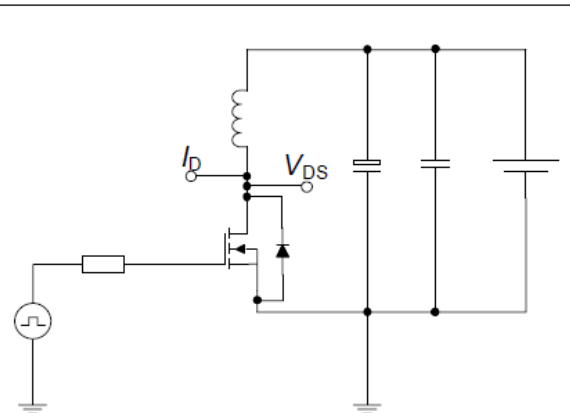
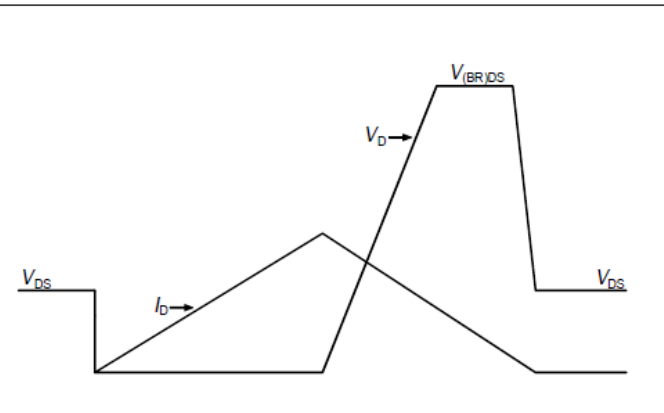
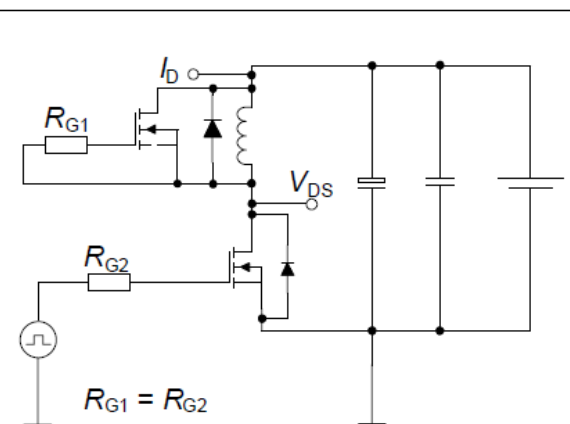
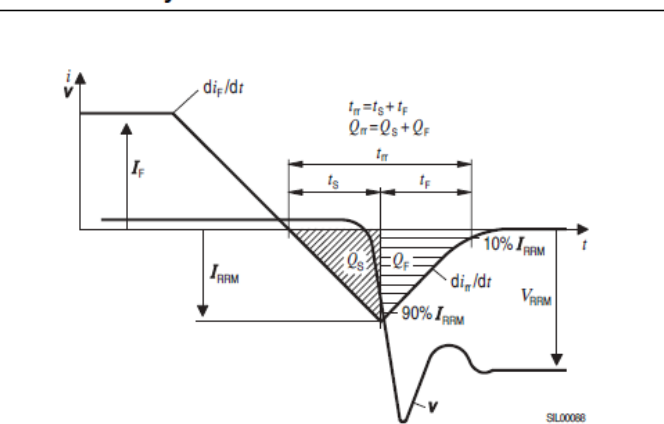
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 22 Test circuit and waveform for diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
 $R_{G1} = R_{G2}$	 $t_{rr} = t_s + t_f$ $Q_{rr} = Q_s + Q_f$ I_{RRM} V_{RRM} $10\% I_{RRM}$ $90\% I_{RRM}$ $10\% V_{RRM}$ $90\% V_{RRM}$ i v di_f/dt t_{rr} t_s t_f Q_s Q_f Q_{rr} $SLD00088$